# REMARKS

Claims 15-119 are pending. In this Response, claims 15, 25 and 28 have been amended.

## I. RESTRICTION REQUIREMENT

A Petition for Withdrawal of Restriction Requirement is filed herewith.

The Examiner asserts that "Applicant's argument that the species including substantially all of the solder joint is within the via hole and the solder joint fills a bottom portion of the via hole without filling the top portion are not patentably distinct is deemed persuasive and the requirement to elect one of these 'species' is withdrawn." (Emphasis added.)

Unfortunately, the Examiner has mischaracterized Applicant's remarks. Applicant stated as follows:

> Species 4A and 4B are not mutually exclusive. That is, substantially all of the solder joint can be within the via hole and the solder joint can fill a bottom portion of the via hole without filling a top portion of the via hole. In fact, that is precisely how solder joint 112 is shown within via hole 104 in Figure 1E. As a result, the claims that read on Species 4A also read on Species 4B and vice-versa. (Emphasis added to "not mutually exclusive.")

Thus, Applicant said nothing about Species 4A and 4B being "not patentably distinct" and wishes to clarify the record.

## II. SECOND 112, FIRST PARAGRAPH REJECTIONS – CLAIMS 57, 58, 67 AND 69

Claims 57, 58, 67 and 69 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement since the claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

The Examiner asserts that in claims 57, 58, 67 and 69, the term "essentially" is undescribed subject matter. This is clearly erroneous.

Claims 57 and 67 recite "essentially all of the solder joint is in the via hole." The Specification reasonably conveys this limitation in Fig. 1E, where essentially all of solder joint 112 is in via hole 104. That is, the vast majority of solder joint 112 is in via hole 104, however a small portion of solder joint 112 extends outside via hole 104 and contacts pad 108. Furthermore, in U.S. Patent No. 6,319,751, the parent case for the captioned-application, claims 55 and 65 recite this limitation, and Examiner Estrada had no problem finding support for this limitation.

Claims 58 and 69 recite "the pad is directly beneath essentially all surface area defined by the via hole after attaching the substrate to the chip." The Specification reasonably conveys this limitation in Fig. 1E, where pad 108 is directly beneath essentially all surface area defined by via hole 104 after attaching substrate 101 to chip 107. That is, the vast majority of pad 108 is directly beneath the surface area defined by via hole 104, however a small portion of pad 108 extends outside (and is not directly beneath) the surface area defined by via hole 104. Furthermore, in U.S. Patent No. 6,319,751, the parent case for the captioned-application, claims 57 and 67 recite this limitation, and Examiner Estrada had no problem finding support for this limitation.

Therefore, Applicant requests these rejections be withdrawn.

## III. SECOND 112, FIRST PARAGRAPH REJECTIONS – CLAIMS 20, 24, 25-30, 35-38, 45-49, 55, 56, 59-61, 66, 68, 70-79, 85-94, 96-104 AND 110-119

Claims 20, 24, 25-30, 35-38, 45-49, 55, 56, 59-61, 66, 68, 70-79, 85-94, 96-104 and 110-119 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement since the claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

The Examiner asserts that in claims 20, 24, 25, 25, 46, 55, 59, 60, 68, 70-79, 85, 86, 90-94, 96-99, 101-104, 111-114 and 116-119, the negative limitations are undescribed subject matter. This is clearly erroneous. The rejections are discussed in individual paragraphs below.

Claim 20 recites "the reflowable material fills a bottom portion of the via hole without filling a top portion of the via hole after the reflowing." The Specification reasonably conveys this limitation in Fig. 1E, where solder joint 112 fills a bottom portion of via hole 104 without filling a top portion of via hole 104. Furthermore, in U.S. Patent No. 6,319,751, the parent case for the captioned-application, claims 27, 48, 55 and 65 recite this limitation (for the reflowable material or the solder joint), and Examiner Estrada had no problem finding support for this limitation. Likewise, in U.S. Patent No. 6,528,891, the sister case for the captioned-application, claims 7 and 17 recite this limitation (for the solder joint), and Examiner Ortiz had no problem finding support for this limitation.

Claim 24 recites "the metallization and the reflowable material are the only materials in the via hole after the reflowing." The Specification reasonably conveys this limitation in Fig. 1E, where copper 105 and solder joint 112 are the only materials in via hole 104 after reflowing solder 106. The Specification also reasonably conveys this limitation in the Substitute Specification at page 6, lines 12-32, which describes providing substrate 1 with plated through-hole copper 105 deposited on the walls of via hole 104 in Fig. 1A, then depositing solder 106 on copper 105 in Fig. 1B, and then reflowing solder 106 to provide solder joint 112 in Fig. 1E. Again, copper 105 and solder joint 112 are the only materials in via hole 104 after reflowing solder 106. Furthermore, in U.S. Patent No. 6,319,751, the parent case for the captioned-application, claims 29, 51, 56 and 66 recite this limitation (for the reflowable material or the solder joint), and Examiner Estrada had no problem finding support for this limitation. Likewise, in U.S. Patent No. 6,528,891, the sister case for the captioned-application, claims 5 and 15 recite this limitation (for the solder joint), and Examiner Ortiz had no problem finding support for this limitation.

Claim 25 recites "applying heat to reflow the solder to form a solder joint that . . . prevents the via hole from exposing the pad." Claim 55 recites similar limitations. The Specification reasonably conveys this limitation in Figs. 1D and 1E, where solder 106 is reflowed to form solder joint 112 that prevents via hole 104 from exposing pad 108. The Specification also reasonably conveys this limitation in the Substitute Specification at page 6, lines 30-32, which describes reflowing solder 106 to form solder joint 112 and firmly join

together via hole 104 and pad 108. Again, solder joint 112 reflows over and covers any portion of pad 108 exposed by via hole 104, and therefore prevents via hole 104 from exposing pad 108. Furthermore, in U.S. Patent No. 6,319,751, the parent case for the captioned-application, claim 54 recites this limitation, and Examiner Estrada had no problem finding support for this limitation.

Claim 46 recites "applying the heat to reflow the solder such that the solder joint fills a bottom portion of the via hole without filling a top portion of the via hole." The Specification reasonably conveys this limitation, as mentioned above for claim 20.

Claim 59 recites "the metallization and the solder joint are the only materials in the via hole after applying the heat." The Specification reasonably conveys this limitation, as mentioned above for claim 24.

Claim 60 recites "depositing solder on the metallization and the bond site, wherein the solder on the metallization is in the via hole, the solder on the bond site is outside the via hole, and the solder on the metallization does not contact the solder on the bond site" and "attaching the substrate to a semiconductor chip, wherein . . . the solder on the bond site does not contact the chip" and "applying heat to reflow the solder such that the solder on the metallization forms a solder joint that contacts and electrically connects the metallization and the pad, [and] the solder on the bond site forms a solder contact that does not contact the solder joint and does not contact the chip." The Specification reasonably conveys these limitation in Fig. 1B, 1D and 1E where solder 106 deposited on copper 105 in via hole 104 does not contact solder 106 deposited on trace 102 in the solder mask opening (Fig. 1B), solder 106 deposited on trace 102 in the solder mask opening does not contact chip 107 (Fig. 1D), and soldering material 113 does not contact solder joint 112 or chip 107 (Fig. 1E). The Specification also reasonably conveys these limitations in the Substitute Specification at page 6, line 12 to page 7, line 3, which describes providing substrate 1 with trace 102 partially covered by solder mask 103 and plated through-hole copper 105 deposited on the walls of via hole 104 in Fig. 1A, then depositing solder 106 on trace 102 at the solder mask opening as well as on copper 105 at via hole 104 in Fig. 1B, then securing chip 107 to substrate 101 such that solder 106 on trace 102 at the solder mask opening

does not contact pad 108 in Fig. 1D, and then reflowing solder 106 to provide solder joint 112 in via hole 104 and soldering material 113 in the solder mask opening such that soldering material 113 does not contact solder joint 112 or chip 107 in Fig. 1E. Again, solder 106 in the solder mask opening (and soldering material 113) does not contact solder 106 in via hole 104 (or solder joint 112), chip 107 or pad 108. Furthermore, in U.S. Patent No. 6,319,751, the parent case for the captioned-application, claim 59 recites this limitation, and Examiner Estrada had no problem finding support for this limitation.

Claim 68 recites "the metallization and the solder joint are the only materials in the via hole after applying the heat to reflow the solder." The Specification reasonably conveys this limitation, as mentioned above for claim 24.

Claim 70 recites "attaching the substrate to the chip using an adhesive that does not electrically connect the substrate and the chip." Claims 71, 75, 76, 85, 86, 90 and 91 recite similar limitations. The Specification reasonably conveys this limitation in Fig. 1D, where adhesive 110 contacts and is sandwiched between the dielectric layer of substrate 101 and the passivation layer of chip 107, but is spaced from copper 105 of substrate 101 and pad 108 of chip 107. The Specification also reasonably conveys this limitation in the Substitute Specification at page 6, lines 24-25, which describes securing chip 107 to substrate 101 by adhesive paste Ablestik Ablebond 961-2. Ablestik Ablebond 961-2 is an electrically insulating epoxy adhesive, as described on the Ablestik Web site (www.ablestik.com) for the Ablebond 961 product. Again, since adhesive 110 is electrical insulator, adhesive 110 does not electrically connect substrate 101 and chip 107. Furthermore, in U.S. Patent No. 6,528,891, the sister case for the captioned-application, claims 21, 22 and 26 recite this limitation (for the assembly), and Examiner Ortiz had no problem finding support for this limitation.

Claim 72 recites "the pad is a bumpless pad." Claims 77, 87 and 92 recite similar limitations. The Specification reasonably conveys this limitation in Fig. 1C, where pad 108 is composed of a Au protective layer on a Ni adhesion layer on a Ti barrier layer on an Al pad. The Specification also reasonably conveys this limitation in the Substitute Specification at page 3, lines 7-11 ("without the need for conventional bumps"), page 3, lines 17-19 ("without external

bumps or wires 24-25"), page 4, line 5 ("The bumpless flip chip assembly of the present invention"), and page 6, lines 21-23 ("These pads 108 are formed with a stake of thin film 109 in the structure of titanium (500 Angstroms)/nickel (700 Angstroms)/gold (1000 Angstroms) to serve as the barrier and adhesive layer"). Again, pads 108 are bumpless. See also the Title: BUMPLESS FLIP CHIP ASSEMBLY WITH SOLDER VIA. Furthermore, in U.S. Patent No. 6,319,751, the parent case for the captioned-application, claims 1 ("A bumpless method") and 54 ("a bumpless terminal pad") recite this limitation, and Examiner Estrada had no problem finding support for this limitation. Likewise, in U.S. Patent No. 6,528,891, the sister case for the captioned-application, claims 23, 25, 28 and 30 recite this limitation, and Examiner Ortiz had no problem finding support for this limitation.

Claim 73 recites "the pad is a solder-free pad." Claims 78, 88 and 93 recite similar limitations. The Specification reasonably conveys this limitation in Fig. 1C, where pad 108 is composed of a Au protective layer on a Ni adhesion layer on a Ti barrier layer on an Al pad. The Specification also reasonably conveys this limitation in the Substitute Specification at page 6, lines 21-23 ("These pads 108 are formed with a stake of thin film 109 in the structure of titanium (500 Angstroms)/nickel (700 Angstroms)/gold (1000 Angstroms) to serve as the barrier and adhesive layer"). Again, pads 108 are solder-free. Furthermore, in U.S. Patent No. 6,528,891, the sister case for the captioned-application, claims 24, 25, 29 and 30 recite this limitation, and Examiner Ortiz had no problem finding support for this limitation.

Claim 74 recites "the pad is a bumpless solder-free pad." Claims 79, 89 and 94 recite similar limitations. The Specification reasonably conveys this limitation, as mentioned above for claims 72 and 73.

Claim 96 recites "the reflowable material is the only material in the via hole that contacts the metallization after the reflowing." The Specification reasonably conveys this limitation in Fig. 1E, where solder joint 112 is the only material in via hole 104 that contacts copper 105 after reflowing solder 106. The Specification also reasonably conveys this limitation in the Substitute Specification at page 6, lines 12-32, which describes providing substrate 1 with plated through-hole copper 105 deposited on the walls of via hole 104 in Fig. 1A, then depositing solder 106 on

copper 105 in Fig. 1B, and then reflowing solder 106 to provide solder joint 112 in Fig. 1E. Again, solder joint 112 is the only material in via hole 104 that contacts copper 105 after reflowing solder 106. Furthermore, in U.S. Patent No. 6,528,891, the sister case for the captioned-application, claims 32 and 37 recite this limitation (for the solder joint), and Examiner Ortiz had no problem finding support for this limitation.

Claim 97 recites "the reflowable material is the only material in the via hole that contacts the pad after the reflowing." The Specification reasonably conveys this limitation in Fig. 1E, where solder joint 112 is the only material in via hole 104 that contacts pad 108 after reflowing solder 106. The Specification also reasonably conveys this limitation in the Substitute Specification at page 6, lines 12-32, which describes providing substrate 1 with plated through-hole copper 105 deposited on the walls of via hole 104 in Fig. 1A, then depositing solder 106 on copper 105 in Fig. 1B, and then reflowing solder 106 to provide solder joint 112 in Fig. 1E. Again, solder joint 112 is the only material in via hole 104 that contacts pad 108 after reflowing solder 106. Furthermore, in U.S. Patent No. 6,528,891, the sister case for the captioned-application, claims 33 and 38 recite this limitation (for the solder joint), and Examiner Ortiz had no problem finding support for this limitation.

Claim 98 recites "the reflowable material is the only material that contacts the metallization and the pad after the reflowing." The Specification reasonably conveys this limitation in Fig. 1E, where solder joint 112 is the only material that contacts copper 105 and pad 108 after reflowing solder 106. The Specification also reasonably conveys this limitation in the Substitute Specification at page 6, lines 12-32, which describes providing substrate 1 with plated through-hole copper 105 deposited on the walls of via hole 104 in Fig. 1A, then depositing solder 106 on copper 105 in Fig. 1B, and then reflowing solder 106 to provide solder joint 112 in Fig. 1E. Again, solder joint 112 is the only material that contacts copper 105 and pad 108 after reflowing solder 106. Furthermore, in U.S. Patent No. 6,528,891, the sister case for the captioned-application, claims 34 and 39 recite this limitation (for the solder joint), and Examiner Ortiz had no problem finding support for this limitation.

Claim 99 recites "the reflowable material is the only conductor external to the chip that contacts the pad after the reflowing." The Specification reasonably conveys this limitation in Fig. 1E, where solder joint 112 is the only conductor external to chip 107 that contacts pad 108 after reflowing solder 106. The Specification also reasonably conveys this limitation in the Substitute Specification at page 6, lines 30-32, which describes reflowing solder 106 to provide solder joint 112 in Fig. 1E. Again, solder joint 112 is the only conductor external to chip 107 that contacts pad 108 after reflowing solder 106. Furthermore, in U.S. Patent No. 6,528,891, the sister case for the captioned-application, claims 35 and 40 recite this limitation (for the solder joint), and Examiner Ortiz had no problem finding support for this limitation.

Claim 101 recites "the solder joint is the only material in the via hole that contacts the metallization." The Specification reasonably conveys this limitation, as mentioned above for claim 96.

Claim 102 recites "the solder joint is the only material in the via hole that contacts the pad." The Specification reasonably conveys this limitation, as mentioned above for claim 97.

Claim 103 recites "the solder joint is the only material that contacts the metallization and the pad." The Specification reasonably conveys this limitation, as mentioned above for claim 98.

Claim 104 recites "the solder joint is the only conductor external to the chip that contacts the pad." The Specification reasonably conveys this limitation, as mentioned above for claim 99.

Claim 111 recites "the solder joint is the only material in the via hole that contacts the metallization." The Specification reasonably conveys this limitation, as mentioned above for claim 96.

Claim 112 recites "the solder joint is the only material in the via hole that contacts the pad." The Specification reasonably conveys this limitation, as mentioned above for claim 97.

Claim 113 recites "the solder joint is the only material that contacts the metallization and the pad." The Specification reasonably conveys this limitation, as mentioned above for claim 98.

Claim 114 recites "the solder joint is the only conductor external to the chip that contacts the pad." The Specification reasonably conveys this limitation, as mentioned above for claim 99.

Claim 116 recites "the solder joint is the only material in the via hole that contacts the metallization." The Specification reasonably conveys this limitation, as mentioned above for claim 96.

Claim 117 recites "the solder joint is the only material in the via hole that contacts the pad." The Specification reasonably conveys this limitation, as mentioned above for claim 97.

Claim 118 recites "the solder joint is the only material that contacts the metallization and the pad." The Specification reasonably conveys this limitation, as mentioned above for claim 98.

Claim 119 recites "the solder joint is the only conductor external to the chip that contacts the pad." The Specification reasonably conveys this limitation, as mentioned above for claim 99.

The M.P.E.P. discusses the written description requirement as follows:

> To satisfy the written description requirement, a patent specification must describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention. (M.P.E.P. § 2163(I), Rev. 2, May 2004, page 2100-164.)
>
> An applicant shows possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention. (M.P.E.P. § 2163(I), Rev. 2, May 2004, page 2100-165.)
>
> While there is no *in haec verba* requirement, newly added claim limitations must be supported in the specification through express, implicit, or inherent disclosure. (M.P.E.P. § 2163(I)(B), Rev. 2, May 2004, page 2100-167.)

> The Examiner, therefore, must have a reasonable basis to challenge the adequacy of the written description requirement. The examiner has the initial burden of presenting by a preponderance of evidence why a person skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims. (M.P.E.P. § 2163.04, Rev. 2, May 2004, page 2100-179.)

The M.P.E.P. also sanctions negative limitations as follows:

> The current view of the courts is that there is nothing inherently ambiguous or uncertain about a negative limitation. So long as the boundaries of the patent protection sought are set forth definitely, albeit negatively, the claim complies with the requirements of 35 U.S.C. 112, second paragraph. (M.P.E.P. § 2173.05(i), Rev. 2, May 2004, page 2100-214.)

The specification need only describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention. Furthermore, the specification can describe the claimed invention using words and figures through express, implicit, or inherent disclosure. There is no *in haec verba* requirement.

Applicant has provided detailed explanations of how the specification describes the negative limitations mentioned above. These detailed explanations establish that the specification describes (and the drawings depict) the negative limitations in sufficient detail that one skilled in the art of semiconductor packaging can reasonably conclude, indeed can readily conclude, that the inventor had possession of the claimed subject matter.

The Examiner now has the burden of presenting by a preponderance of evidence why a person skilled in the art of semiconductor packaging would not recognize that the specification reasonably conveys these negative limitations. This burden cannot be met.

Therefore, Applicant requests these rejections be withdrawn.

## IV. SECOND 112, FIRST PARAGRAPH REJECTIONS – CLAIMS 15, 16, 18-20, 22-30, 35-38, 45-49, 55, 56, 59-61, 66, 68, 70-79, 85-104 AND 110-119

Claims 15, 16, 18-20, 22-30, 35-38, 45-49, 55, 56, 59-61, 66, 68, 70-79, 85-104 and 110-119 are rejected under 35 U.S.C. § 112, first paragraph, as based on a disclosure which is not enabling.

The Examiner asserts that claims 57, 58, 67 and 69 recite essential limitations preceded by the term "essentially," however claims 15, 16, 18-20, 22-30, 35-38, 45-49, 55, 56, 59-61, 66, 68, 70-79, 85-104 and 110-119 fail to recite these essential limitations, and a claim which omits matter disclosed to be essential to the invention as described in the specification or in other statements of record may be subject to rejection under Section 112. This is clearly erroneous.

Claims 57 and 67 recite "essentially all of the solder joint is in the via hole," and claims 58 and 69 recite "the pad is directly beneath essentially all surface area defined by the via hole after attaching the substrate to the chip."

Thus, claims 57, 58, 67 and 69 recite "essentially" as relative terminology. Claims 57, 58, 67 and 69 say nothing about these limitations being "essential" to the claimed invention. The Examiner's attempt to twist the term "essentially" from relative terminology into an admission of an "essential" limitation is illogical and improper.

Therefore, Applicant requests these rejections be withdrawn.

## V. SECTION 102 REJECTIONS – HINO ET AL.

Claims 15, 16, 18-20, 22-27, 29, 30, 36-38, 45-49, 70-79 and 95-104 are rejected under 35 U.S.C. § 102(e) as being anticipated by *Hino et al.* (U.S. Patent No. 6,157,084).

*Hino et al.* discloses semiconductor device 1 that includes anisotropic conductive film carrier 2, semiconductor element 3 and insulating resin 4. Film carrier 2 includes conductive circuit 5, flexible insulator layer 6, conductive paths 7 and 8, and bumps 9 and 10. Conductive circuit 5 is embedded in insulator 6, conductive path 7 and bump 9 extend from conductive

circuit 5 to surface 6a of insulator layer 6, and conductive path 8 and bump 10 extend from conductive circuit 5 to surface 6b of insulator layer 6. Semiconductor element 3 includes electrode 12, and bump 9 contacts electrode 12.

Claims 15 and 25 have been amended to recite "the metallization . . . extends along the walls to the first and second surfaces."

*Hino et al.* fails to teach or suggest this approach, as the Examiner apparently recognizes in not rejecting claim 28 over *Hino et al.*

Under 35 U.S.C. § 102, anticipation requires that each and every element of the claimed invention be disclosed in the prior art. *Akzo N.V. v. United States International Trade Commission*, 1 USPQ 2d 1241, 1245 (Fed. Cir. 1986), *cert. denied*, 482 U.S. 909 (1987). That is, the reference must teach every aspect of the claimed invention. See M.P.E.P. § 706.02.

Therefore, Applicant requests that these rejections be withdrawn.

## VI. SECTION 103 REJECTIONS – HINO ET AL. AND GAYNES ET AL.

Claim 40 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Hino et al.* in view of *Gaynes et al.* (U.S. Patent No. 6,165,885).

*Gaynes et al.* listed in the Notice of References Cited is U.S. Patent No. 6,002,177 rather than 6,165,885.

At any rate, Applicant submits this rejection is moot for the reasons set forth above for claim 25.

## VII. FIRST INFORMATION DISCLOSURE STATEMENT

A First Information Disclosure Statement accompanied by a PTO-1449 was filed on May 10, 2001. A copy of the Return Postcard establishing PTO receipt of the Information Disclosure Statement is attached. However, the Office Action did not include an initialed copy of the PTO-1449. Therefore, Applicant requests that the next written communication to Applicant include an initialed copy of the PTO-1449.

## VIII. SECOND INFORMATION DISCLOSURE STATEMENT

A Second Information Disclosure Statement accompanied by a PTO-1449 was filed on January 28, 2002. A copy of the Return Postcard establishing PTO receipt of the Information Disclosure Statement is attached. However, the Office Action did not include an initialed copy of the PTO-1449. Therefore, Applicant requests that the next written communication to Applicant include an initialed copy of the PTO-1449.

## IX. SUBSTITUTE SPECIFICATION

A Substitute Specification was filed on May 10, 2001. A copy of the Return Postcard establishing PTO receipt of the Substitute Specification is attached. However, the Office Action fails to acknowledge the Substitute Specification. Furthermore, in U.S. Patent No. 6,319,751, the parent case for the captioned-application, Examiner Estrada had no problem entering the Substitute Specification. Likewise, in U.S. Patent No. 6,528,891, the sister case for the captioned-application, Examiner Ortiz had no problem entering the Substitute Specification. Therefore, Applicant requests that the next written communication to Applicant confirm that the Substitute Specification has been entered.

## X. DRAWING CHANGES

A Submission of Proposed Drawing Amendment for Approval by Examiner was filed on May 10, 2001. A copy of the Return Postcard establishing PTO receipt of the Submission is attached. However, the Office Action fails to acknowledge the Submission. Furthermore, in U.S. Patent No. 6,319,751, the parent case for the captioned-application, Examiner Estrada had no problem approving the proposed drawing changes. Likewise, in U.S. Patent No. 6,528,891, the sister case for the captioned-application, Examiner Ortiz had no problem approving the proposed drawing changes. Therefore, Applicant requests that the next written communication to Applicant approve the proposed drawing changes.

## XI. MISCELLANEOUS

The Office Action cover sheet and the footer on pages 2-14 indicate Art Unit 2822. However, the Examiner is with Art Unit 2827. Applicant mentions this to point out a potential glitch that may cause confusion in other cases.

## XII. CONCLUSION

In view of the remarks set forth herein, the application is believed to be in condition for allowance. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 27, 2004

D Sigmond — 9/27/04

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Respectfully submitted,

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